REMARKS

Claim Status

Currently, claims 1-10 are pending. No amendments were made.

Claim Rejections – 35 USC §102

In paragraphs 2 - 12 of the Office Action, the Examiner rejected claims 1-10 under 35 USC §102(b) as being anticipated by Saueret *et al.* (US Patent 5,951,704). For at least the reasons set out below, Applicants traverse.

The present invention is directed to a method for testing an emulated logical circuit, wherein: a model of the logical circuit is loaded with a hardware description language into an emulator; the emulated circuit is set into an operational mode in which some or all of the flip-flops included therein are functionally chained into shift registers by means of interfacing additional logic elements; and the structural arrangement of the logic circuit in the hardware emulator is compared with the structural arrangement of the model of the logic circuit. For such a purpose, test patterns are applied to inputs of the emulator or the shift registers and clocked through the shift registers. At the outputs of the emulator or the shift registers, a check is performed to determine whether the received result matches the expected result. Results of the check are then used for the comparison between the structural arrangement of the logic circuit in the hardware emulator and the structural arrangement of the model of the logic circuit in order to recognize the corresponding error source (i.e. planning error, defect of the hardware emulator, etc.) responsible for an incorrect operation of the model of the logical circuit. The present invention is further directed to a device for performing the method according to the invention.

In contrast to the present invention, Saueret discloses a test system emulator with emulator software for emulating hardware in a test system for semiconductors, wherein the emulator software comprises: an emulating unit for emulating the hardware unit of the test system; a component group emulator which emulates the functionality of the semiconductor element to be tested; a unit for collecting data; and a component test emulator which generates a test signal applied to the component emulator.

Saueret, however, does not teach nor suggest that the emulated logical circuit is set into an operating mode, in which some or all of the flip-flops contained therein

are functionally chained into shift registers by means of interfacing additional logic elements. Because of this chaining, the functioning of the logical circuit to be tested can be tested relatively simple and readily, and it can further be determined whether the structural arrangement of the logical circuit in the hardware emulator is comparable or identical with the structural arrangement of the modeled logical circuit.

In addition, the present invention is based on a standard hardware emulator which has a plurality of gates whose parameters can be set wherein the gates can be arbitrarily connected (see page 1, lines 21-*et seq.*). In contrast, Saueret is based only on software components which form the system, as is discussed in claim 1 and col. 10, lines 33-35.

Accordingly, Saueret does not disclose all the limitations of the present invention and is therefore unavailable as a §102(b) reference. For at least the above reasons, reconsideration and withdrawal of the rejection is respectfully requested.

CONCLUSION

The present response is intended to correspond with the Revised Amendment Format. Applicants understand that with the Revised Amendment Format, the provisions of 37 CFR §1.121 are waived. Should any part of the present response not be in full compliance with the requirements of the Revised Amendment Format, the Examiner is asked to contact the undersigned for immediate correction.

No new matter has been added by way of the aforementioned amendments.

In the event that the transmittal form is separated from this document and the Patent Office determines that an extension of time and/or other relief is required, Applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees in connection with the filing of this document to **Deposit Account No.: 502464** referencing **client reference: 2002P15288WOUS**. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Date: 10/12/2005

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